AMENDMENT AND RESPONSE UNDER 37 CFR §1.111   Page 3
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Title: A SEGMENTED BRANCH PREDICTOR

IN THE CLAIMS

Please amend the claims as follows:

1.   (Original) An apparatus comprising:

        storage means for storing a first type of branch history information;

        intermediate prediction means for generating a plurality of intermediate branch
prediction results based off of a plurality of portions of the store branch history
information, wherein the intermediate prediction means uses a portion of the branch
history information that is smaller than all of the branch history information stored within
the storage means in order to generate the plurality of intermediate branch prediction
results;

        final prediction means for generating a final branch prediction result based off of
the plurality of intermediate branch prediction results.

2.   (Original) The apparatus of claim 1 wherein the storage means is a register within a
microprocessor.

3.   (Original) The apparatus of claim 1 wherein the storage means is a memory location
within a computer system.

4.   (Original) The apparatus of claim 1 wherein the intermediate prediction means comprises
a plurality of intermediate branch predictors to perform a plurality of intermediate branch
predictions in parallel.

5.   (Original) The apparatus of claim 1 wherein the final prediction means is a single branch
predictor.

6.   (Original) The apparatus of claim 1 wherein the intermediate branch prediction means
comprises a first plurality of intermediate branch prediction units to perform a plurality of branch
predictions in parallel, and a second plurality of intermediate branch prediction units to perform

a plurality of branch predictions in series with the first plurality of intermediate branch prediction units.

7.   (Currently Amended) A computer system comprising:

a memory unit to store a first and second ~~plurality of~~ instructions;

a processor to predict whether to execute the first or the second ~~plurality of~~ instructions based, at least in part, on an intermediate branch prediction to be made by a plurality of intermediate branch prediction units, the intermediate branch ~~history~~ prediction units each corresponding to a different portion of a set of branch history information, each different portion being smaller than the set of branch history information.

8.   (Original) The computer system of claim 7 wherein the processor comprises a final branch prediction unit to perform a final branch prediction based on predictions of the intermediate branch prediction units.

9.   (Original) The computer system of claim 8 further comprising a branch history storage unit to store the set of branch history information.

10.   (Original) The computer system of claim 9 wherein the branch history storage unit is a memory location.

11.   (Original) The computer system of claim 9 wherein the branch history storage unit is a register within the processor.

12.   (Original) A processor comprising:

a storage unit for storing a first type of branch history information;

a plurality of intermediate prediction units to generate a plurality of intermediate branch prediction results based off of a plurality of portions of the store branch history information, wherein each intermediate prediction unit uses a portion of the branch

history information that is smaller than all of the branch history information stored within

the storage unit in order to generate the plurality of intermediate branch prediction

results.

13.   (Original) The processor of claim 12 further comprising a final prediction unit to generate

a final branch prediction result based off of the plurality of intermediate branch prediction

results.

14.   (Original) The processor of claim 13 wherein the storage unit is a register within a

microprocessor.

15.   (Original) The processor of claim 13 wherein the storage unit is a memory location

within a computer system.   •

16.   (Original) The processor of claim 13 wherein the intermediate prediction units are to

perform a plurality of intermediate branch predictions in parallel.

17.   (Original) The processor of claim 13 wherein the intermediate branch prediction units

comprise a first plurality of intermediate branch prediction units to perform a plurality of branch

predictions in parallel, and a second plurality of intermediate branch prediction units to perform

a plurality of branch predictions in series with the first plurality of intermediate branch prediction

units.

18.   (Currently Amended) A method comprising:

          accessing a plurality of branch prediction segments in parallel;

          performing a plurality of intermediate branch predictions based off of the plurality

of branch prediction segments, wherein each intermediate branch prediction is based off

of a different branch prediction segment and each branch prediction segment is smaller

than the sum of the branch prediction segments; and

          generating a signal to indicate a final branch predication.

19.   (Original) The method of claim 18 further comprising performing a final branch prediction based off of the plurality of intermediate branch predictions.

20.   (Currently Amended) A machine-readable medium comprising instructions, which if executed by a machine, cause the machine to perform a method comprising:

       accessing a plurality of branch prediction segments in parallel;

       performing a plurality of intermediate branch predictions based off of the plurality of branch prediction segments, wherein each intermediate branch prediction is based off of a different branch prediction segment and each branch prediction segment is smaller than the sum of the branch prediction segments; and

       generating a signal to indicate a final branch predication.

21.   (Original) The machine-readable medium of claim 20 further comprising performing a final branch prediction based off of the plurality of intermediate branch predictions.